2. Amendments to the Claims:

A clean version of the entire set of pending claims (including amendments to the claims, if any) is submitted herewith per 37 CFR § 1.121(c)(3). This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently amended) Switched mode power supply assembly ~~(1)~~ comprising:

at least two switched mode power supply units ~~(10_i)~~ coupled to each other in parallel~~;~~, each power supply unit ~~(10_i) having~~ comprising a window comparator and an output stage ~~(50_i, 60_i)~~, the window comparator being configured to generate mode switch control signals by comparing an output signal from the output stage to at least one signal boundary level, and the output stage being configured to ~~capable of~~ selectively ~~operating~~ operate in a first mode wherein ~~its~~ the output signal ~~($I_{OUT,i}$)~~ is increasing and operating in a second mode wherein ~~its~~ the output signal ~~($I_{OUT,i}$)~~ is decreasing in response to the mode switch control signals; and

a control device ~~(100)~~ receiving the mode switch control signals from ~~all~~ the at least two power supply units ~~(10_i)~~;

wherein the control device ~~(100), if it finds that the actual phase relationship between two power supply units deviates from an optimal phase relationship,~~ is designed to generate synchronising control signals for at least one power supply unit ~~(10_2)~~ when an actual phase relationship between the at least one power supply unit and another power supply unit deviates from an optimal phase relationship, effectively changing ~~the~~ timing of at least one mode switch moment, such that the deviation between the actual phase relationship and said optimal phase relationship is reduced.

2. (Currently amended) Switched mode power supply assembly ~~(1)~~ comprising:

a plurality of ~~at least two~~ switched mode power supply units ~~(10_i)~~ coupled to each other in parallel~~;~~, each power supply unit ~~(10_i) having~~ comprising:

an output stage ~~(50$_i$, 60$_i$)~~ for generating an output signal ~~($I_{OUT,i}$)~~, the output stage ~~(50$_i$, 60$_i$)~~ being capable of selectively operating in a first mode wherein the output signal ~~($I_{OUT,i}$)~~ is increasing and operating in a second mode wherein the output signal ~~($I_{OUT,i}$)~~ is decreasing; and

~~each power supply unit (10$_i$) having~~ mode switch control means ~~(30$_i$)~~ for generating a first mode switch control signal ~~(Ri)~~ for controlling the output stage ~~(50$_i$, 60$_i$)~~ to switch from ~~its~~ the first operating mode to ~~its~~ the second operating mode, and for generating a second mode switch control signal ~~(Si)~~ for controlling the output stage ~~(50$_i$, 60$_i$)~~ to switch from ~~its~~ the second operating mode to ~~its~~ the first operating mode; and

~~the switched mode power supply assembly (1) further comprising~~ a control device ~~(100) having~~ comprising inputs ~~(121, 122, 123, 124)~~ for receiving the mode switch control signals from all of the plurality power supply units ~~(10$_i$)~~;

wherein the control device ~~(100)~~ is designed to determine an optimal phase relationship between ~~the~~ phases of the mode switch control signals of one power supply unit ~~(10$_2$)~~ and ~~the~~ phases of the mode switch control signals of ~~at least one~~ a reference power supply unit ~~(10$_1$)~~;

wherein the control device ~~(100)~~ is designed to compare the phases of the mode switch control signals of said one power supply unit ~~(10$_2$)~~ with the phases of the mode switch control signals of said ~~at least one~~ reference power supply unit ~~(10$_1$)~~ to determine an actual phase relationship; and

wherein the control device ~~(100), if it finds that the actual phase relationship deviates from said optimal phase relationship,~~ is designed to generate synchronising control signals for at least one of said one power supply unit ~~(10$_2$)~~ and ~~/or~~ said ~~at least one~~ reference power supply unit ~~(10$_1$)~~ when it finds that the actual phase relationship deviates from the optimal phase relationship, effectively changing the timing of at least one mode switch moment of at least one of said one power supply unit ~~(10$_2$)~~ and ~~/or of~~ said ~~at least one~~ reference power supply unit ~~(10$_1$)~~, respectively, such that the deviation between the actual phase relationship and said optimal phase relationship is reduced, in order to ensure interleaved operation of all of the plurality of power supply units.

3. (Currently amended) Switched mode power supply assembly ~~(1)~~ according to claim 2, wherein the control device ~~(100), if it finds that said one power supply unit (10_2) is lagging with respect to said optimal phase relationship,~~ is designed to generate a delaying synchronising control signal ~~($SCDH_1$, $SCDL_1$)~~ for said ~~at least one~~ reference power supply unit ~~(10_1)~~ when it finds that said one power supply unit is lagging with respect to said optimal phase relationship, effectively delaying the timing of at least one mode switch moment of said ~~at least one~~ reference power supply unit ~~(10_1)~~.

4. (Currently amended) Switched mode power supply assembly ~~(1)~~ according to claim 2, wherein the control device ~~(100), if it finds that said one power supply unit (10_2) is lagging with respect to said optimal phase relationship,~~ is designed to generate an advancing synchronising control signal ~~($SCAH_2$, $SCAL_2$)~~ for said one power supply unit ~~(10_2)~~ when it finds that said one power supply unit is lagging with respect to said optimal phase relationship, effectively advancing the timing of at least one mode switch moment of said one power supply unit ~~(10_2)~~.

5. (Currently amended) Switched mode power supply assembly ~~(1)~~ according to claim 2, wherein the control device ~~(100), if it finds that said one power supply unit (10_2) is early with respect to said optimal phase relationship,~~ is designed to generate a delaying synchronising control signal ~~($SCDH_2$, $SCDL_2$)~~ for said one power supply unit ~~(10_2)~~ when it finds that said one power supply unit is early with respect to said optimal phase relationship, effectively delaying the timing of at least one mode switch moment of said one power supply unit ~~(10_2)~~.

6. (Currently amended) Switched mode power supply assembly ~~(1)~~ according to claim 2, wherein the control device ~~(100), if it finds that said one power supply unit (10_2) is early with respect to said optimal phase relationship,~~ is designed to generate an advancing synchronising control signal ~~($SCAH_1$, $SCAL_1$)~~ for said ~~at least one~~ reference power supply unit ~~(10_1)~~ when it finds that said one power supply unit is early with respect to said optimal

phase relationship, effectively advancing the timing of at least one mode switch moment of said ~~at least one~~ reference power supply unit ~~(10_1)~~.

7. (Currently amended) Switched mode power supply assembly ~~(1)~~ according to claim 2, wherein the control device ~~(100)~~ is designed to generate its synchronising control signals such that the phase mismatch is completely compensated in one step.

8. (Currently amended) Switched mode power supply assembly ~~(1)~~ according to claim 2, wherein the control device ~~(100)~~ is designed to generate its synchronising control signals such that the phase mismatch is reduced by a predetermined constant factor K2.

9. (Currently amended) Switched mode power supply assembly ~~(1)~~ according to claim 2, wherein the control device ~~(100)~~ is designed to calculate a first time difference ~~(|t21 - t13|)~~ between a first time ~~(t21)~~ when the output signal ~~(SM2)~~ of said one power supply unit ~~(10_2)~~ reaches a first boundary level ~~(S_{BH})~~ and a second time ~~(t13)~~ when the output signal ~~(SM1)~~ of said ~~at least one~~ reference power supply unit ~~(10_1)~~ reaches the same first boundary level ~~(S_{BH})~~;

wherein the control device ~~(100)~~ is designed to calculate a second time difference ~~(|t23 - t13|)~~ between said second time ~~(t13)~~ and a third time ~~(t23)~~ when the output signal ~~(SM2)~~ of said one power supply unit ~~(10_2)~~ reaches said first boundary level ~~(S_{BH})~~ again;

wherein the control device ~~(100)~~ is designed to calculate the difference between said first time difference ~~(|t21 - t13|)~~ and said second time difference ~~(|t23 - t13|)~~;

wherein the control device ~~(100)~~ is designed to divide said calculated difference by a predetermined factor ~~(K2)~~ to yield a delay time ~~(|t31 - t23|)~~; and

wherein the control device ~~(100)~~ is designed to generate a delaying synchronising control signal ~~($SCDH_2$)~~ for said one power supply unit ~~(10_2)~~ such that said one power supply unit ~~(10_2)~~ switches its operating mode at a delayed switching time ~~(t31)~~ calculated as ~~the~~ said third time ~~(t23)~~ plus said delay time ~~(|t31 - t23|)~~.

10. (Currently amended) Switched mode power supply assembly ~~(1)~~ according to claim 2, wherein the output stage ~~(50$_i$, 60$_i$)~~ of each power supply unit comprises at least one input ~~(R; S)~~ coupled to an output of an AND gate ~~(141, 142)~~, ~~this~~ the AND gate ~~(141, 142)~~ ~~having~~ comprising an input receiving a command signal ~~(R1; S1)~~ from the corresponding mode switch control means ~~(30$_i$)~~ and ~~having~~ another input receiving a delaying synchronising control signal ~~(SCDH1, SCDL1)~~ from the control device ~~(100)~~.

11. (Currently amended) Switched mode power supply assembly ~~(1)~~ according to claim 2, wherein the output stage ~~(50$_i$, 60$_i$)~~ of each power supply unit comprises at least one input ~~(R; S)~~ coupled to an output of an OR gate ~~(161, 162)~~, ~~this~~ the OR gate ~~(161, 162)~~ ~~having~~ comprising an input receiving a command signal ~~(R1; S1)~~ from the corresponding mode switch control means ~~(30$_i$)~~ and ~~having~~ another input receiving an advancing synchronising control signal ~~(SCAH1, SCAL1)~~ from the control device ~~(100)~~.

12. (Currently amended) Switched mode power supply assembly ~~(1)~~ according to claim 2, wherein all of the power supply units ~~(10)~~ are mutually identical.

13. (Currently amended) Switched mode power supply assembly ~~(1)~~ according to claim 2, wherein each power supply unit ~~(10$_i$)~~ further comprises a target signal input ~~(16$_i$)~~, all of the target signal inputs of all of the power supply units being connected in parallel to one common target signal source ~~(S_{TARGET})~~.

14. (Currently amended) Switched mode power supply assembly ~~(1)~~ according to claim 2, wherein each power supply unit ~~(10$_i$)~~ further comprises a current output ~~(13$_i$)~~, all of the current outputs of all of the power supply units being connected in parallel to one common assembly output ~~(3)~~.

15. (Currently amended) Switched mode power supply assembly ~~(1)~~ according to claim 2, wherein each power supply unit ~~(10$_i$)~~ further comprises a first supply input ~~(11$_i$)~~ and a second supply input ~~(12$_i$)~~, all of the first supply inputs of all of the power supply units being

connected in parallel to one common high voltage supply source ~~(V_{HIGH})~~, and all of the second supply inputs of all of the power supply units being connected in parallel to one common low voltage supply source ~~(V_{LOW})~~.

16. (Currently amended) Switched mode power supply assembly ~~(1)~~ according to claim 2, wherein ~~said signal generating means comprise~~ the output stage of each power supply unit comprises:

two controllable switches ~~(61, 62)~~ coupled in series between a first supply input ~~(11)~~ and a second supply input ~~(12)~~, a node ~~(A)~~ between said switches being coupled to ~~said~~ a module output ~~(13)~~;

a switch driver ~~(50) having~~ comprising outputs ~~(52, 53)~~ respectively coupled to control inputs of ~~respective~~ the switches ~~(61, 62)~~, the switch driver ~~(50)~~ being capable of operating in a first operative state in which it generates ~~its~~ control output signals such that the second switch ~~(62)~~ is non-conductive while the first switch ~~(61)~~ is in ~~its~~ a conductive state, and being capable of operating in a second operative state in which it generates ~~its~~ control output signals such that the first switch ~~(61)~~ is non-conductive while the second switch ~~(62)~~ is in ~~its~~ a conductive state; and wherein the mode switch control means of each power supply unit comprises:

a window comparator ~~(30) having~~comprising a high boundary input ~~(32)~~ and a low boundary input ~~(33)~~, a control output ~~(34)~~ coupled to a control input ~~(51)~~ of said switch driver ~~(50)~~, and a measuring signal input ~~(36)~~ coupled to receive ~~said~~ a measuring signal ~~(S_M)~~ from ~~said~~ a current sensor ~~(67)~~;

wherein the window comparator ~~(30)~~ is adapted to generate a first control signal commanding said switch driver ~~(50)~~ to enter ~~its~~ the first operative state when said ~~falling~~ measuring signal ~~(S_M)~~ becomes equal to ~~the~~ a low signal level ~~(S_{BL})~~ at ~~its~~ a low boundary input ~~(33)~~ of the measuring signal, and to generate a second control signal commanding said switch driver ~~(50)~~ to enter ~~its~~ the second operative state when said ~~rising~~ measuring signal ~~(S_M)~~ becomes equal to ~~the~~ a high signal level ~~(S_{BH})~~ at ~~its~~ a high boundary input ~~(32)~~ of the measuring signal.

17. (Currently amended) Switched mode power supply assembly ~~(1)~~ according to claim 2, wherein the mode switch control means ~~(30_i)~~ are designed for generating a first mode switch control signal ~~(Ri)~~ controlling the output stage ~~(50_i, 60_i)~~ to switch from ~~its~~ the first operating mode to ~~its~~ the second operating mode ~~if~~ when the ~~rising~~ output signal ~~($I_{OUT,i}$)~~ ~~reaches~~ rises to a first boundary level ~~(S_{BH})~~ and for generating a second mode switch control signal ~~(Si)~~ controlling the output stage ~~(50_i, 60_i)~~ to switch from ~~its~~ the second operating mode to ~~its~~ the first operating mode ~~if~~ when the ~~falling~~ output signal ~~($I_{OUT,i}$)~~ ~~reaches~~ falls to a second boundary level ~~(S_{BL})~~.

18. (Currently amended) Switched mode power supply assembly ~~(1)~~ according to claim 1, wherein the power supply modules are implemented as DC/DC converter modules.

19. (Currently amended) mode power supply assembly ~~(1)~~ according to claim 1, wherein the power supply modules are implemented as DC/AC inverter modules.

20. (Currently amended) Solar cell assembly, comprising a boost converter for up-converting the output voltage of the solar cells, having ~~its~~ an output voltage coupled to a DC/AC inverter, wherein at least one of ~~either~~ said boost converter or said inverter~~, or both, comprise~~ comprises a switched mode power supply assembly ~~(1)~~ according to claim 1.

21. (Currently amended) Driver for driving a lamp such as a gas discharge lamp, comprising a switched mode power supply assembly ~~(1)~~ according to claim 1 as a DC/AC inverter for generating supply current for the lamp.

22. (Currently amended) Actuator for a motion control apparatus, comprising a switched mode power supply assembly ~~(1)~~ according to claim 1.